

Figure 1

CEBus Chirp

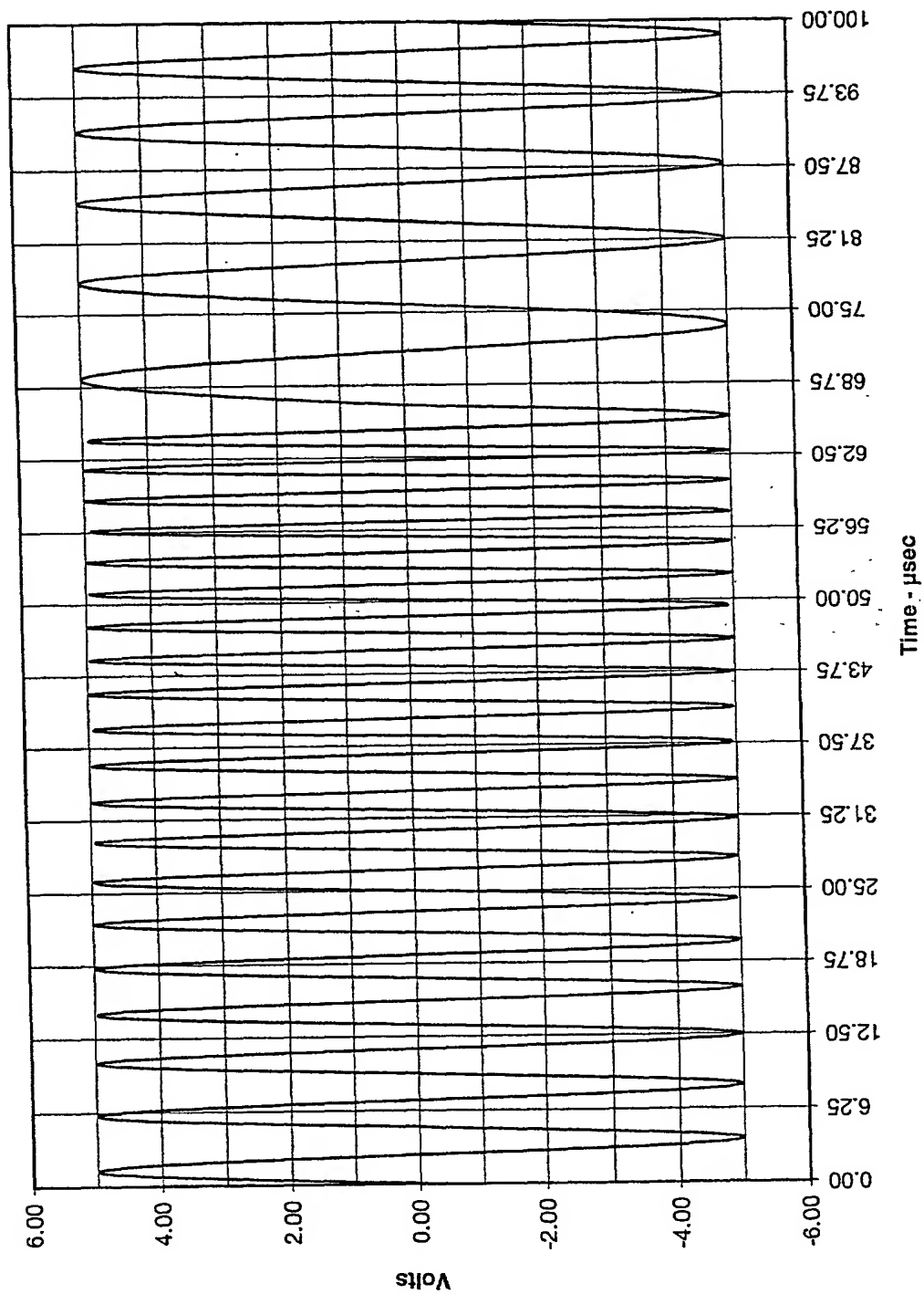


Figure 2

Shifted CEBus Chirp

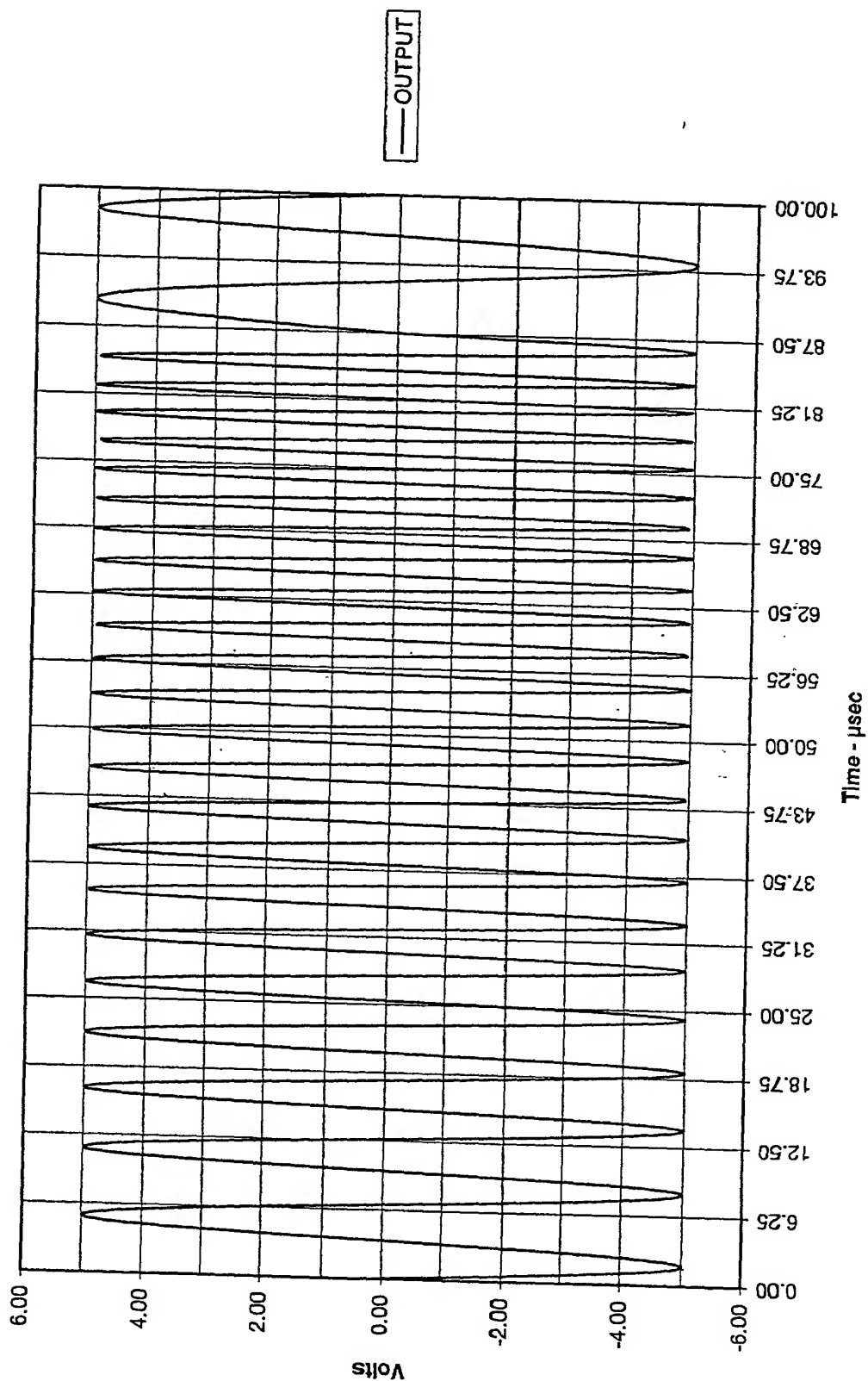


Figure 3

Shifted CEBus Chirp

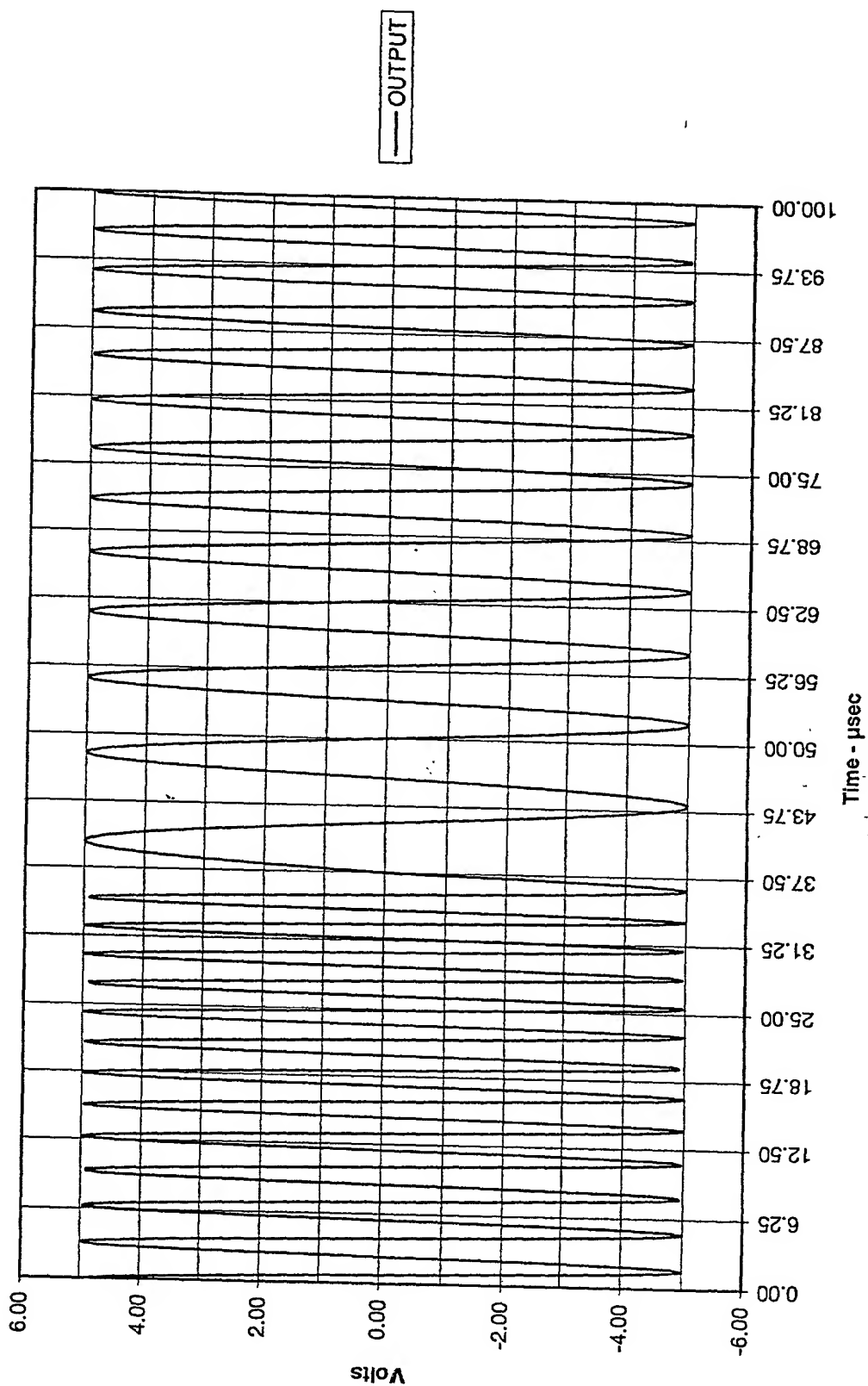


Figure 4

Superschirp

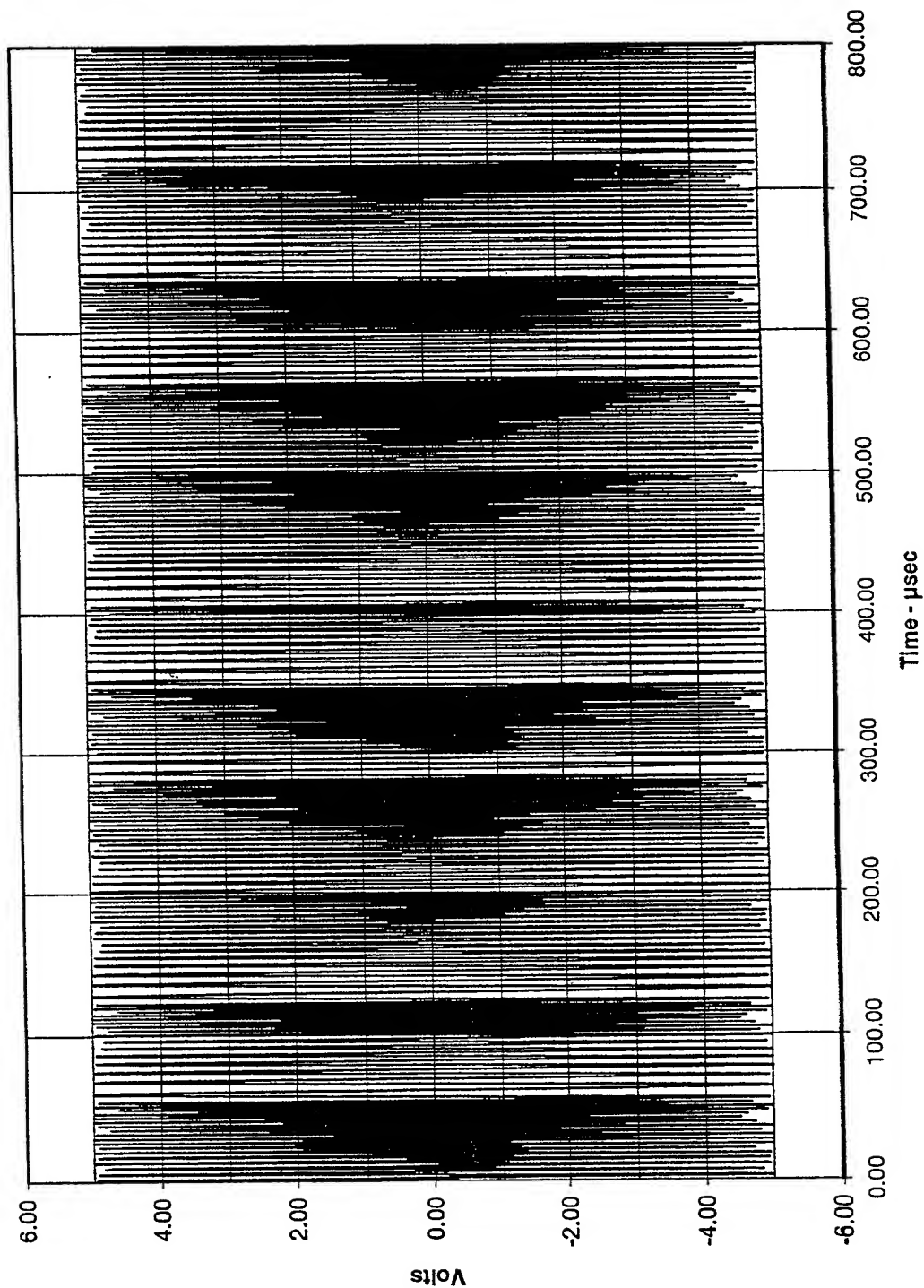


Figure 5

Shifted Superchirp

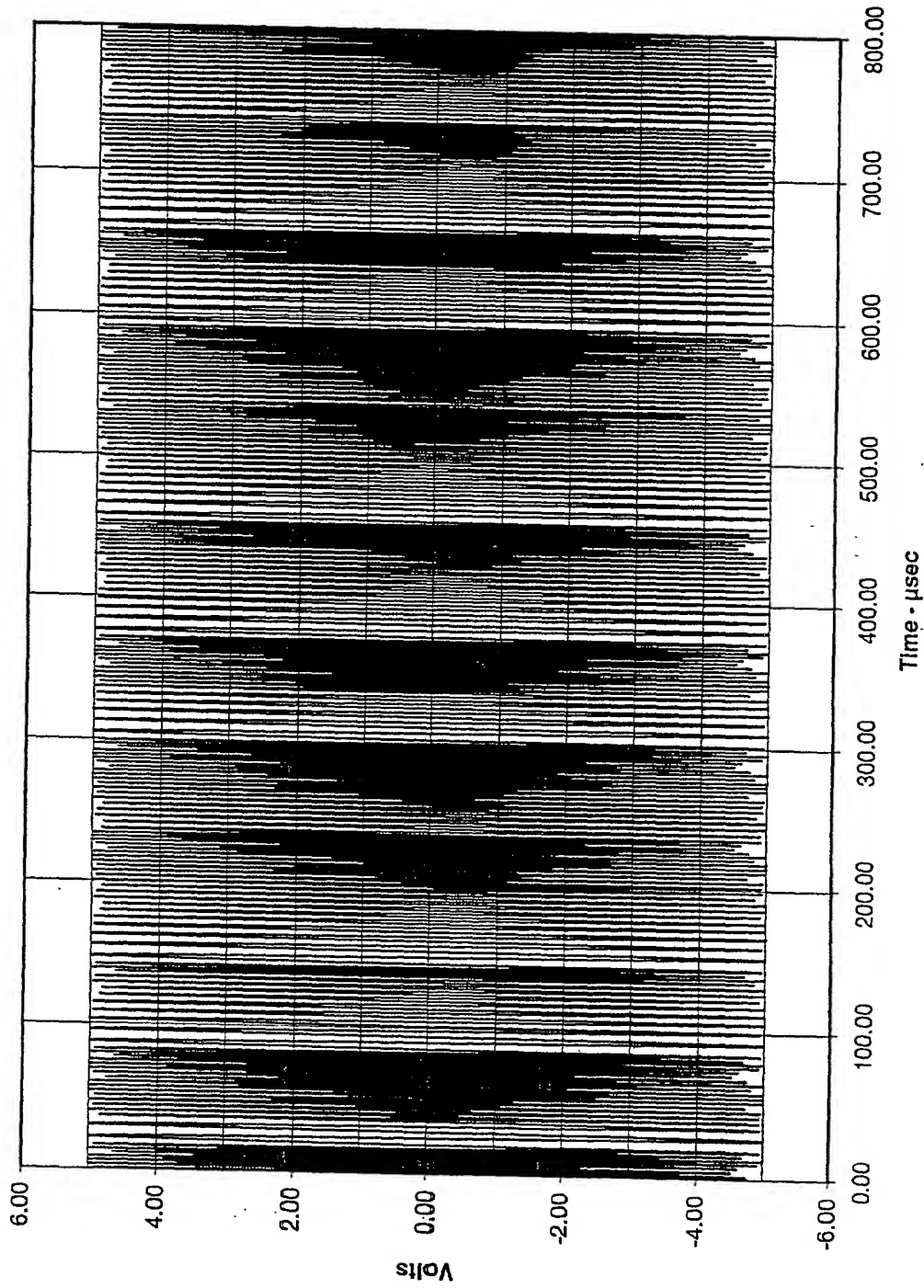
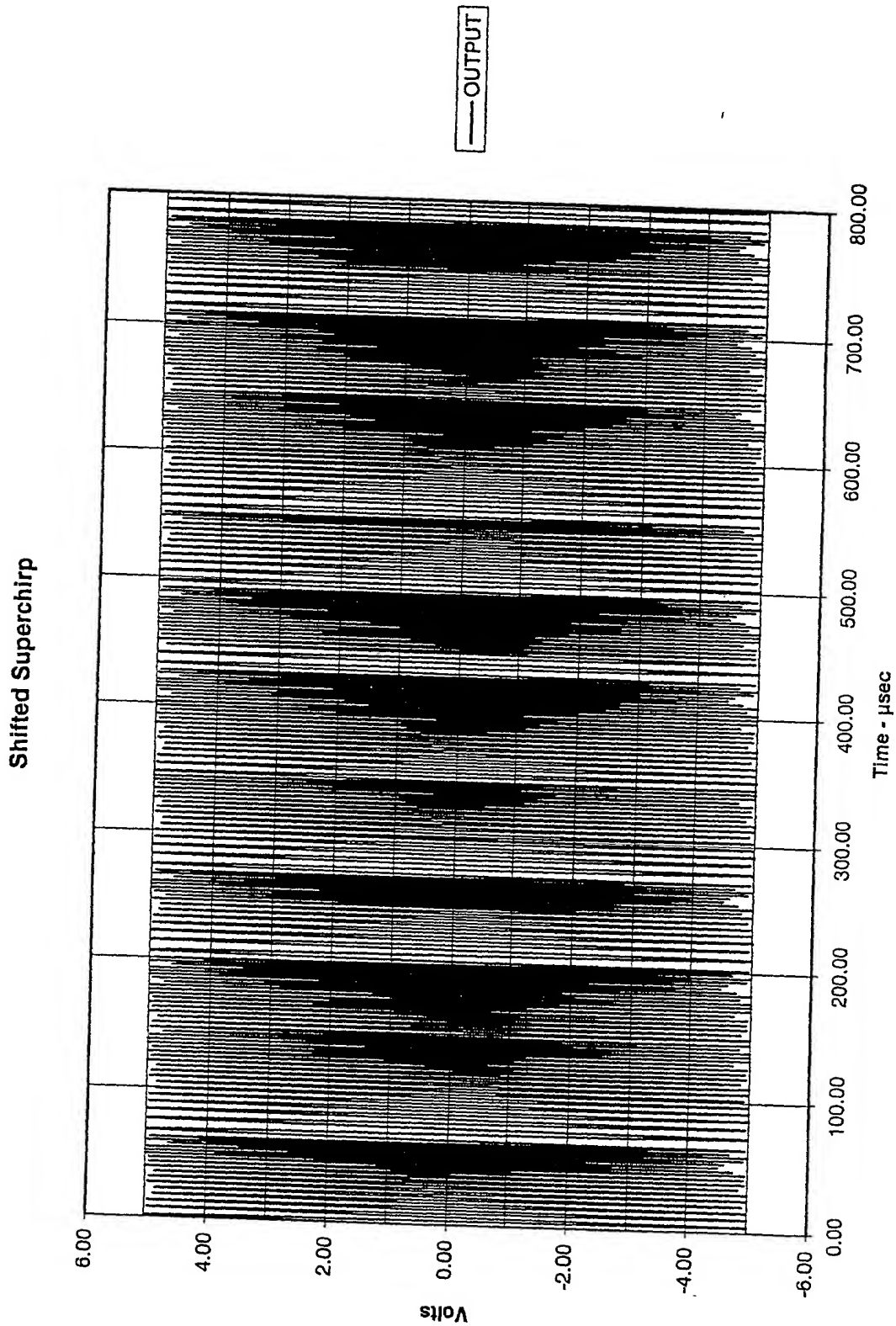


Figure 6



Received Shifted Superchirp

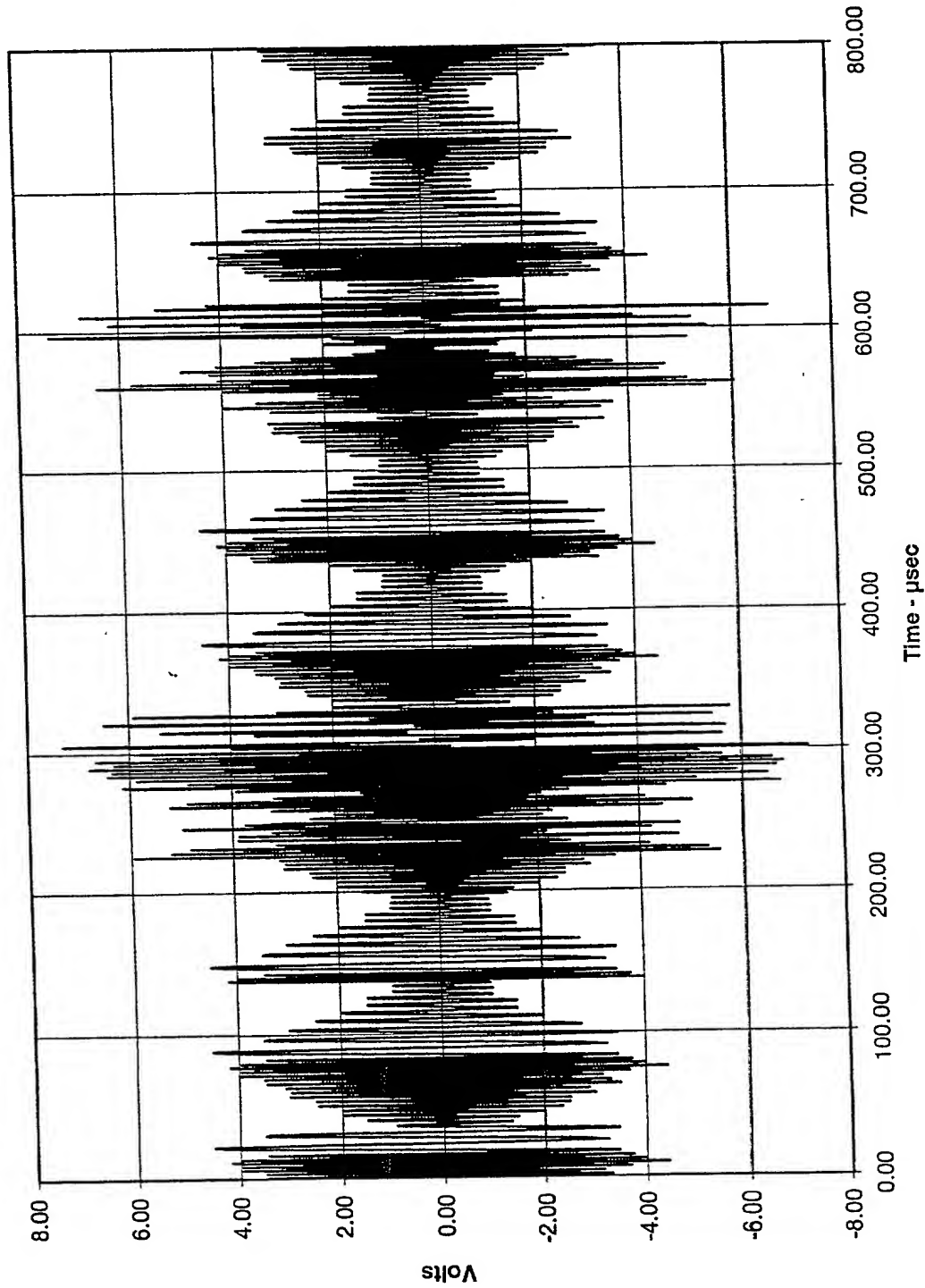
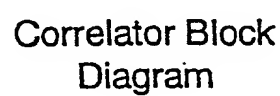


Figure 8



► 8-bit Data

Figure 10

Zero-Crossing Detector
Block Diagram

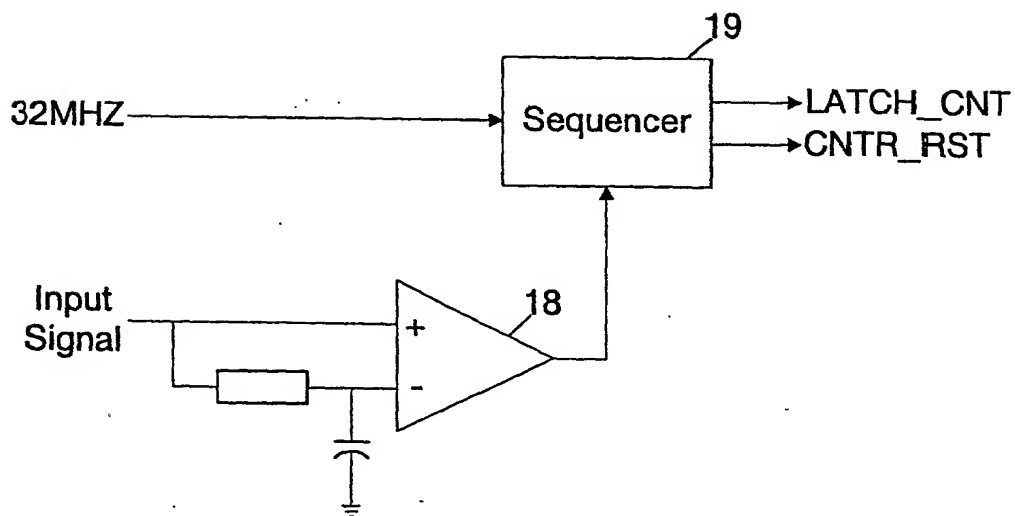


Figure 11

Cycle Period Measurement Module
Block Diagram

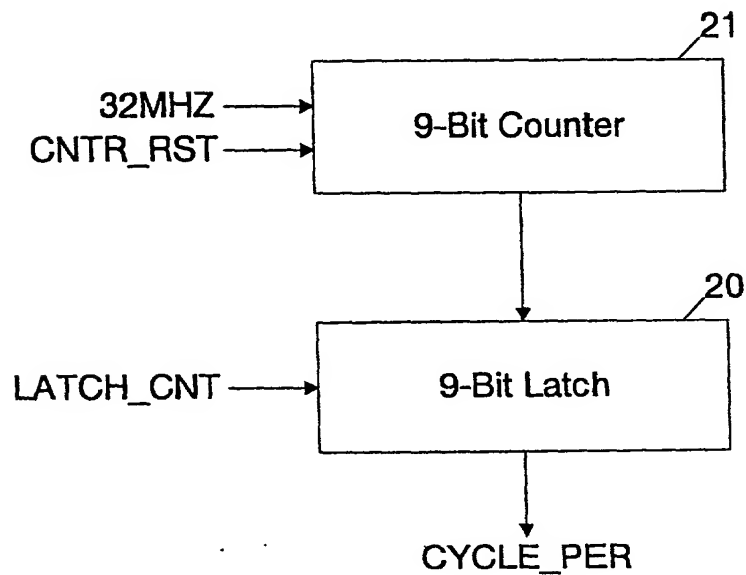


Figure 12

Elapsed Time Counter
Block Diagram

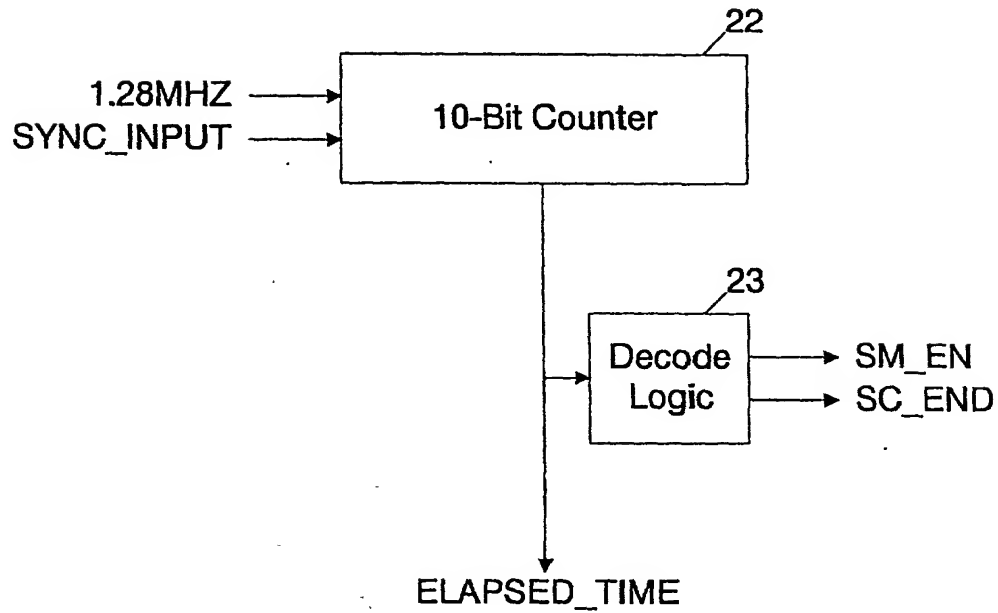
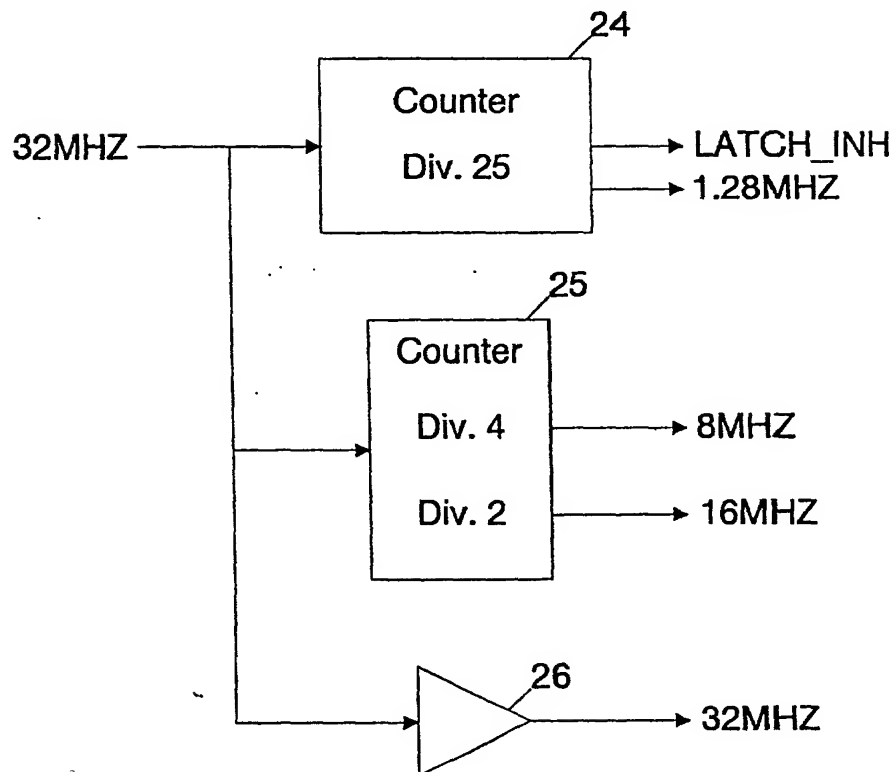


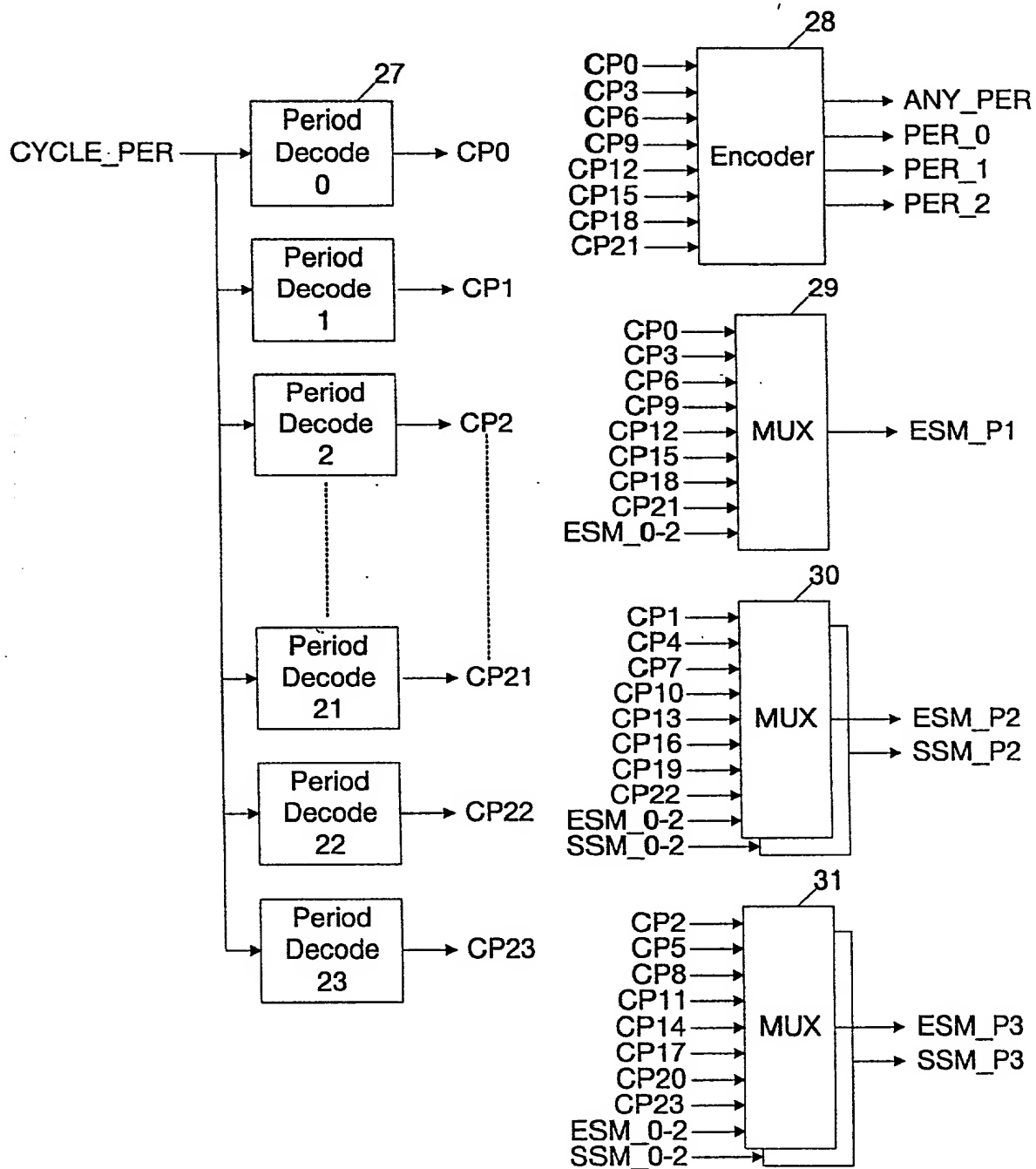
Figure 13

Clock Generator
Block Diagram



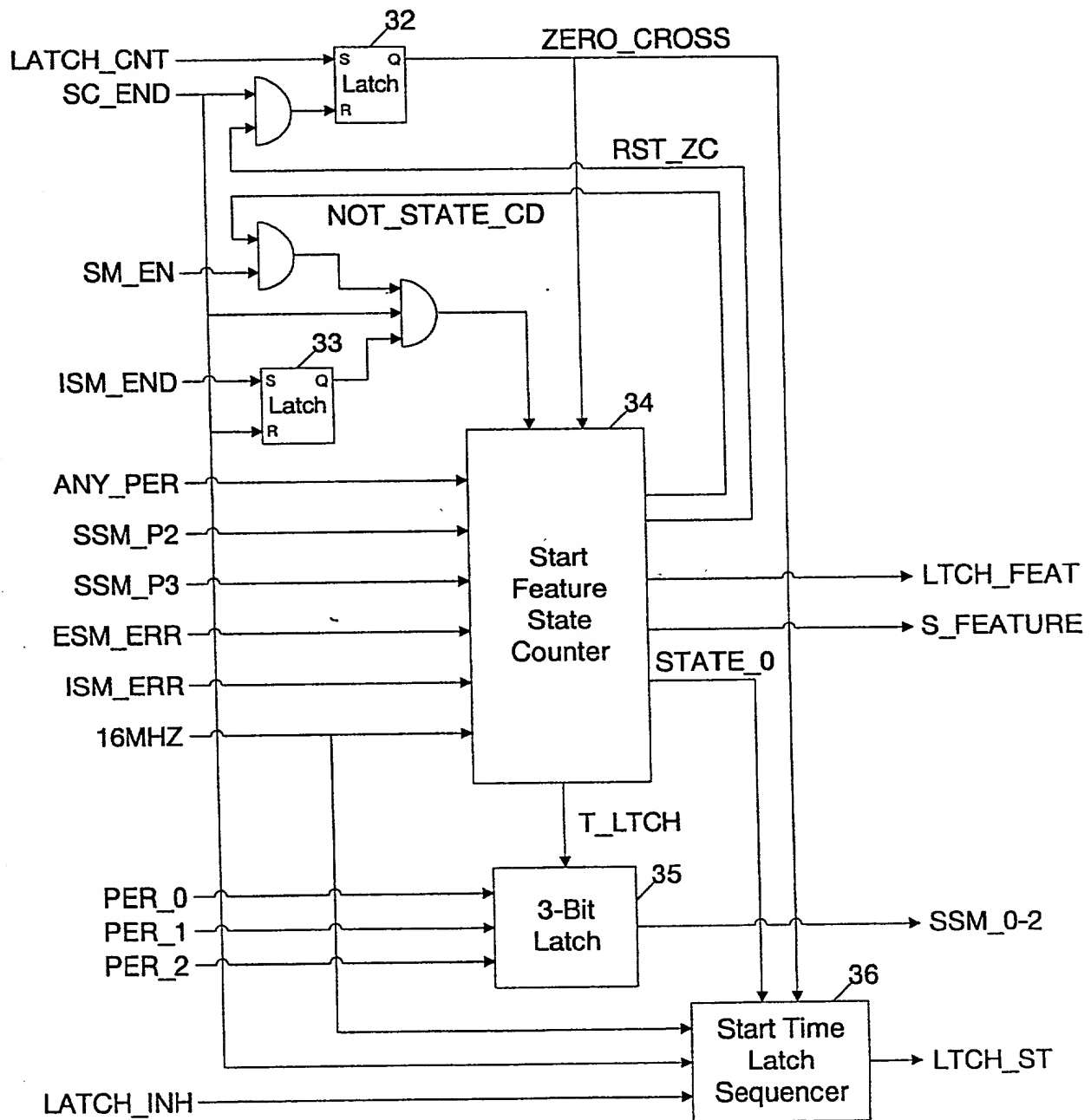
Period Detector Block Diagram

Figure 14



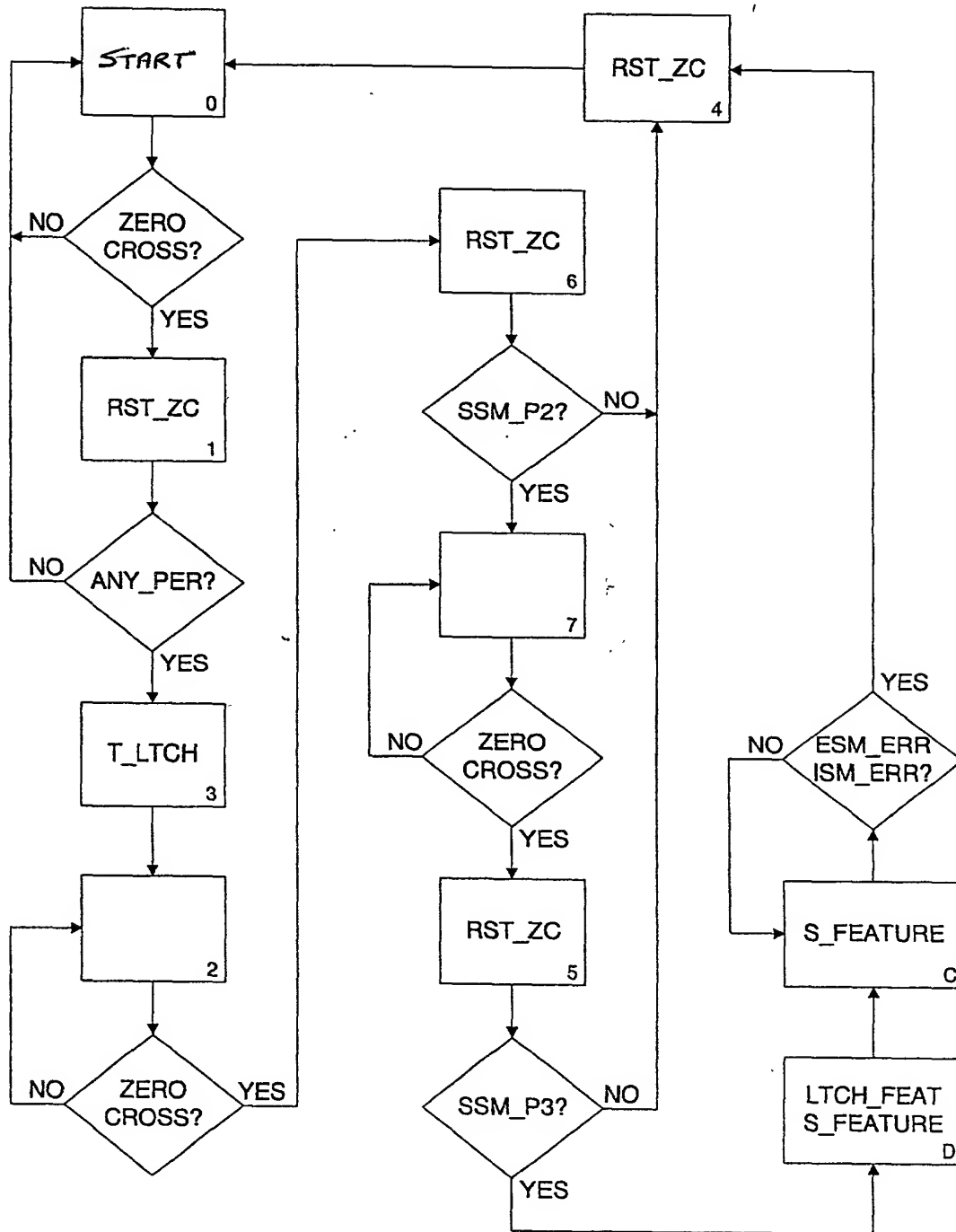
Start Feature State Machine Block Diagram

Figure 15



Start Feature State Machine State Diagram

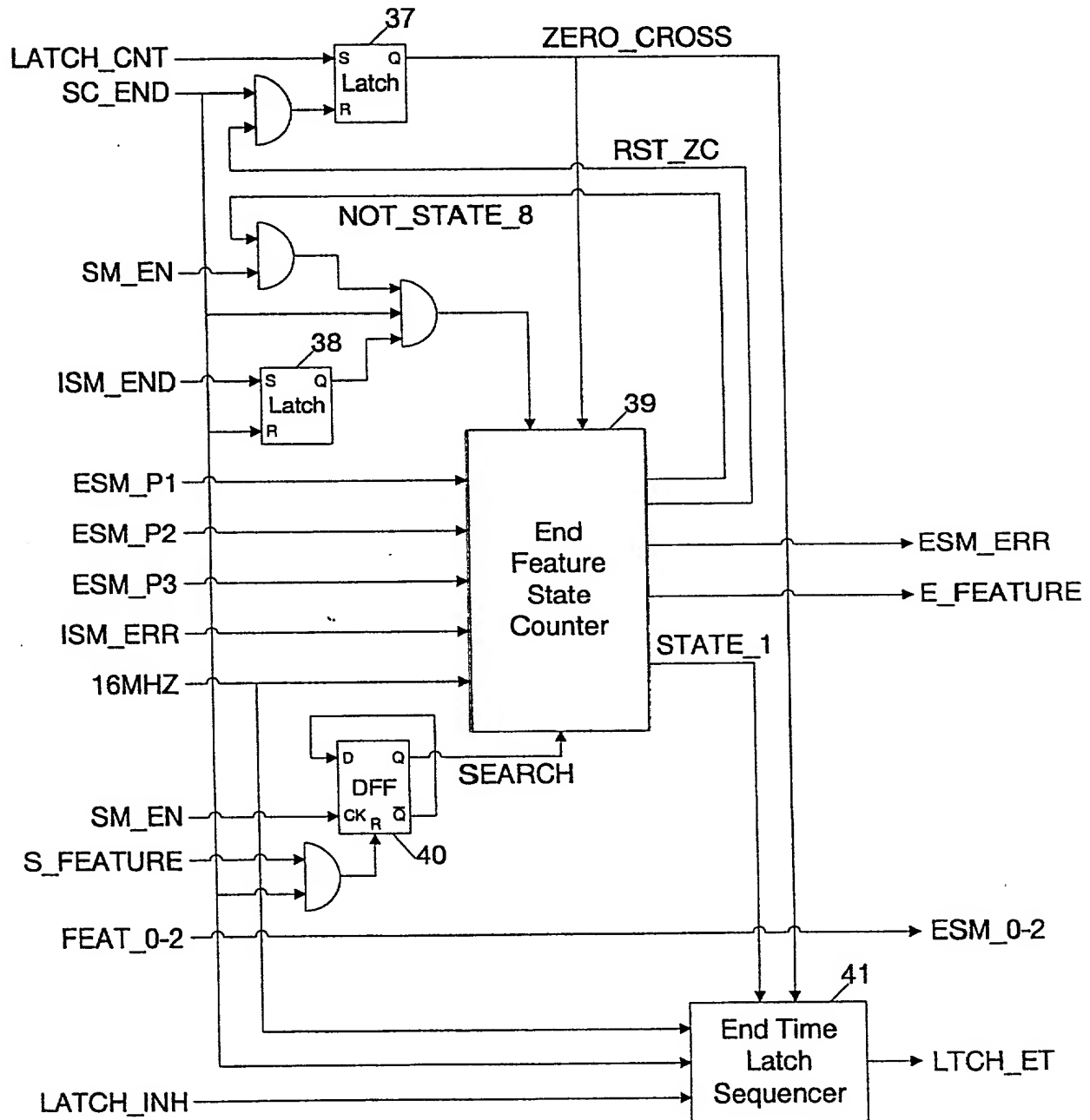
Figure 16



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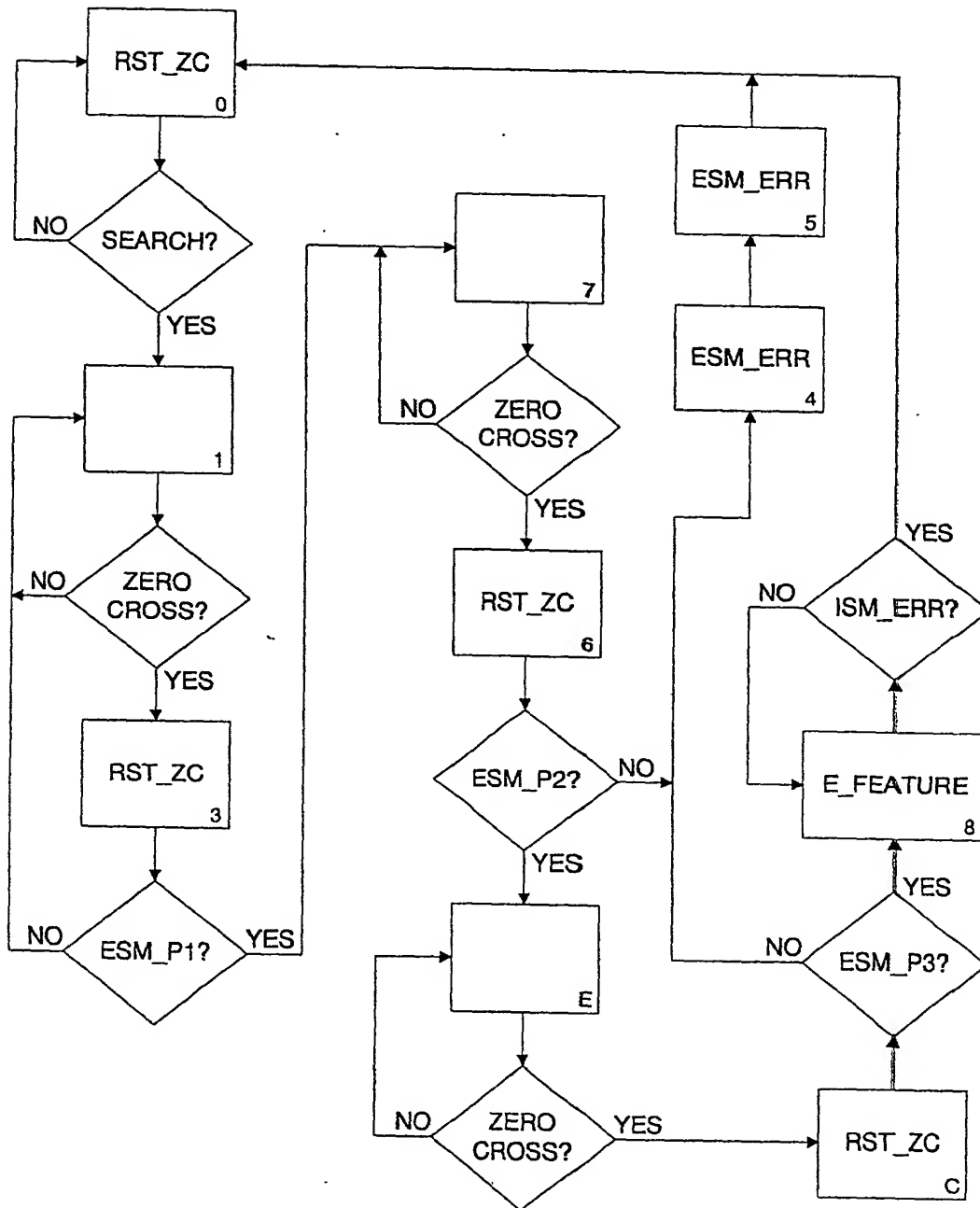
End Feature State Machine Block Diagram

Figure 17



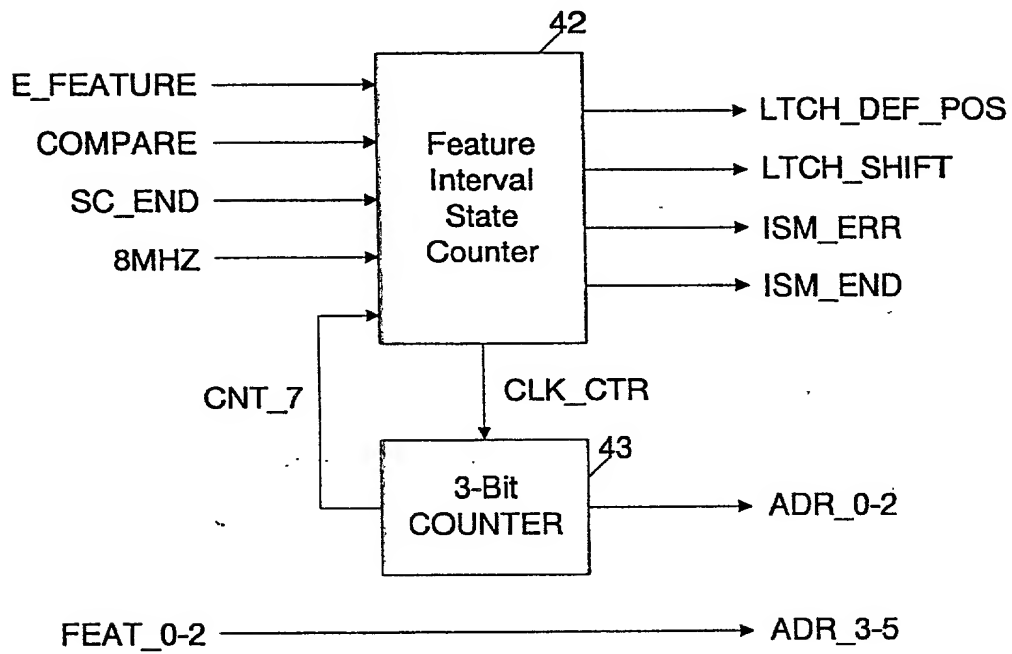
End Feature State Machine State Diagram

Figure 18



Feature Interval State Machine Figure 19

Block Diagram



Feature Interval State Machine State Diagram

Figure 20

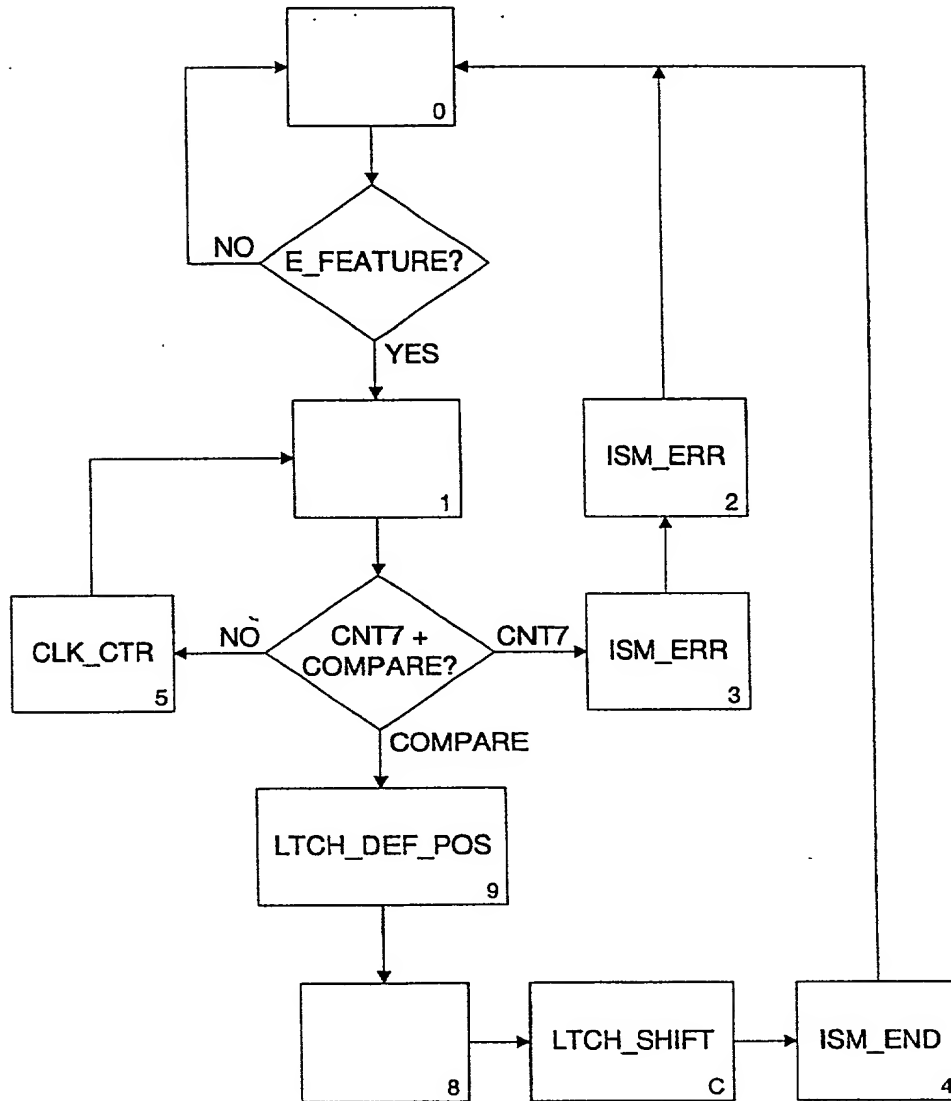


Figure 21

Comparator
Block Diagram

